



FPGA Xilinx

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Frequently Asked Questions

Non-Confidential

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Contents

1 FPGA Xilinx FAQs.....	6
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1 FPGA Xilinx FAQs

Here are answers to common questions about Arm Cortex-M processors with Xilinx-based FPGAs and SoCs.

Watch this [on-demand webinar](#) to learn how to use the Arm Cortex-M1 and Cortex-M3 soft IP for no cost in Xilinx FPGAs. The webinar will take you through the key steps you need to take to develop a successful FPGA-based device, including integration and software development.

If you want to get started using Cortex-M processors with Xilinx, explore the webinar FAQs below for more information.

Are there any license fees for deploying an Arm Processor per device?

No royalties, no license fees. These cores are completely free!

Why are the Arm processors free?

Arm did this to address demand from our customers, and because we believe that choice is a good thing - the commercial FPGA market is growing and OEMs want to scale their product across different platforms, selecting the best fit for their design requirements. It makes sense for people to build on an architecture that you can maintain across the design spectrum as requirements evolve, reusing software and expertise, but there aren't that many architectures out there that offer that.

It's no doubt a win-win for us and developers: they can speed up design and integrate industry-leading technology easily - which is good for them - and yet they do it on Arm, which is great for the ecosystem.

Which FPGA families support these IP cores?

While the example projects are currently available for Diligent's Arty-S7 and Arty-A7 boards, these processors can be used on ANY Xilinx device, 7-series, or newer, so long as you have available logic resources. Also expect resource utilization rates to be similar across Xilinx families. As shown in the webinar, Arm Cortex-M processors also make ideal co-processors in a Zynq-7000 (Arm Cortex-A9) or Zynq UltraScale+ (Arm Cortex-A53 and Cortex-R5) devices.

What versions of the Vivado and SDK were used?

Vivado and Xilinx SDK 2019.2 are recommended for evaluating and implementing Arm Cortex-M soft CPU IP. Vivado and Xilinx SDK provide a unified tool set for design and programming all Xilinx (7 series, or newer) devices. Vivado 2018.3 can be used by upgrading the project from 2018.2. Additionally, for Artix-7 and Spartan-7 devices, Xilinx provides a free version of Vivado called Vivado WebPACK. To see which devices are supported by Vivado WebPack, [click here](#) for UG973 (see Table 2-1). As shown in the [webinar](#), board files and example projects are found for many of our boards. The board files provide data to Vivado that specify what components and interfaces are available on each board. Thus, IP can be added quickly without having to reference data sheets and schematics. Example projects are available for select boards that provide easy-to-use starting points for new designs. And all of these example projects are completely configurable.

What version of Keil MDK was used and what is the cost?

Keil MDK-Lite, uVision 5 was used for this demo. This is free for software design up to 32KB applications. Also, DesignStart FPGA offers Keil MDK Essential as a 90-day free trial. For more details, visit [MDK Microcontroller Development Kit](#)

How does the MicroBlaze processor compare to the Arm Cortex-M processors?

MicroBlaze is Xilinx's soft-processor core solution. It's a 32-bit RISC architecture and is highly configurable. Certain MicroBlaze configurations can run as fast as 200+MHz in some devices. In the smallest configuration, both Arm Cortex-M1 and MicroBlaze are optimized and are roughly about the same size. Arm's rich ecosystem provides incredible resources including tool vendors, libraries and more, making it a valuable addition to the Xilinx IP portfolio. Also, MicroBlaze is not being replaced by Arm Cortex-M IP processors. MicroBlaze will be available for many years to come.

Is PetaLinux supported on Arm Cortex-M processors?

PetaLinux is only supported for MicroBlaze and Zynq-based devices.

When will you have FreeRTOS and lwIP BSP support?

FreeRTOS is scheduled for the 2019.2 release later this year. lwIP support is provided as an available library for bare-metal applications and FreeRTOS.

Are other Arm processors available for Xilinx devices? For example, the Cortex-M4 CPU?

At this time, only the Arm Cortex-M1 and Cortex-M3 processors as soft CPU IP are available through DesignStart FPGA. Arm Cortex-M processors also make ideal co-processors in a Zynq-7000 (Arm Cortex-A9) or Zynq UltraScale+ (Arm Cortex-A53 and Cortex-R5) devices.

Is it possible to debug this soft IP Arm using JTAG?

At this time, this feature is unavailable. However, it is something we are investigating and hope to provide a solution soon. Until then, the Arm DAPLink board provides the debug interface. Alternatively, JTAG pins can be connected to the FPGA I/O pins, (not the dedicated JTAG pins that are used for programming). If you then have a suitable header connected to those FPGA I/O pins, then you can debug with your chosen JTAG debugger.

When will Xilinx SDK support programming Cortex-M processors?

Script support should be available by early summer 2019 and XSDK GUI support by late 2019.

How much internal memory is available for code storage and execution?

Each Xilinx device has available local memory called block RAM. The density of available block RAM per device scales with device logic density. For example, the Spartan-7 XC7S25 has over 200KB of internal memory! If more memory is needed, you can either move to a large device or add external memory, such as DDR memory. Currently our [Github](#) has repositories for Boards and Example Projects, however we are considering one for IP as well.

Which AXI version is supported for Arm Cortex-M processors?

The Cortex-M1 and Cortex-M3 processors natively support AHB. Arm adds an AXI shim that works with the Xilinx interconnects. Thus AMBA-3 and AMBA-4 are supported. Xilinx IP libraries also support AMBA-3 IP as AHB and APB bridges are available in the IP catalog.

What security measures does Xilinx offer?

Nearly every Xilinx device offers bitstream encryption and authentication. Only two Spartan-7 devices, XC7S6 and XC7S15, do not offer integrated security blocks. See our [FPGA Design Security page](#) for more information.

What is the power consumption of these devices?

For FPGAs, power consumption is determined by device logic density. So bigger devices will consume more power. Smaller Spartan-7 devices can run under 50mW. And Xilinx's [Power Estimator](#) can provide insight not only for power estimation, but also guidance on power supply design!

What is a BSP?

Board Support Package. This is a set of files that provide low-level drivers for all the hardware. This allows for a consistent interface between high-level software projects, and the low-level hardware drivers. The package will incorporate the memory map, for example, extracting the locations as consistently named variables.

Are there plans to support AXF files natively in Vivado?

Not in Vivado, however, AXF files can be programmed directly into the board from Keil MDK via the DAPlink debug adapter. In the webinar, we showed an alternative flow without using the debug interface, rather the Xilinx JTAG interface.

How do I change the external pin locations of this design or use this example project on another board?

Pin locations are controlled by the project's XDC constraint file. The Digilent boards also use a board file that defines all the ports available on their board and allows an easy connection using Vivado IP Integrator. For your own boards, you can specify your own pinout. [See this video](#) on how to configure Vivado pin constraints.

If you want to use one of these example projects on another board, you can change this target device in the Vivado project settings and select the board or device you intend to target. Note: all of your existing pin constraints will be invalid. You must change these to match your board pinout. Also, if changing Xilinx architecture, some of the internal IP may need to be changed to match the desired architecture, for example clocking resources.

Is it possible to do RTL simulation of the entire block design (including the initialized block RAMs with elf binary) with either the Vivado simulator or Mentor Questa?

Yes, both Vivado simulator and Questa are supported. The example design comes with scripts and instructions as to how to run these simulations including using your own compiled code.

Is bit-banding supported?

Bit-banding is available for the Cortex-M3 as a configuration option.

Is the Arm source code available?

All the source code for this design and the software are available. The code for Cortex-M1 and Cortex-M3 CPUs is encrypted.

What safety features are available from Xilinx?

Please refer to our [Functional Safety webpage](#).

Why are these cores not integrated into Xilinx devices like the Cortex-A9 in Zynq-7000?

As you can see, the size of these cores is quite small thus they are easy to implement in Xilinx logic. And this enables customers to use as many of these cores as they require in their design.

Do these IP processors have an FPU?

No. Cortex-M1 and Cortex-M3 CPUs don't have an FPU. However, MicroBlaze does offer an FPU option. And Zynq-based devices with Cortex-A processors, such as the Zynq-7000 family, features an FPU unit.